Integrated Circuit Design for High-Speed Frequency Synthesis

by

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This book is now available, as of February 2006, and as expected, some errors are being found. If you find errors in this book, or have comments about this book, please send email to cp {at} doe {dot} carleton {dot} ca. A list of errors, comments, etc will be posted. If you would rather not be acknowledged on the errata list, let us know and your name will not appear. Comments in blue have been added since the last version of the errata updated on March 10, 2007.

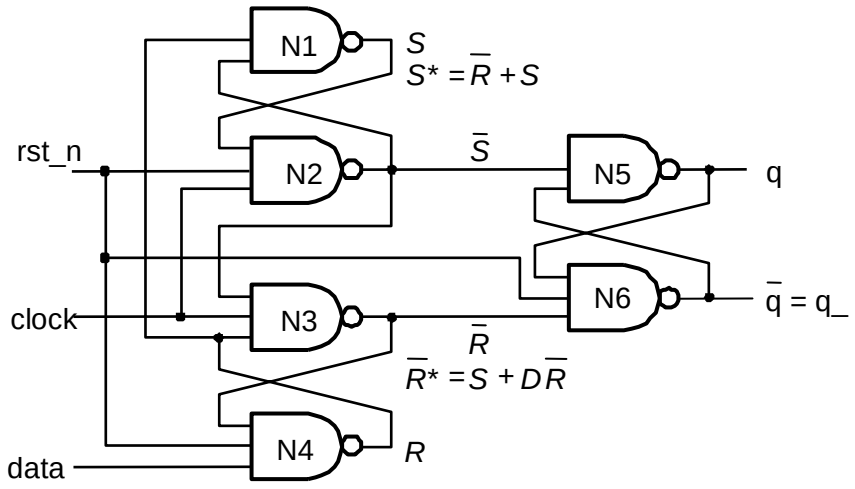
Page 17 In Section 2.2, page 17, The sentence, “Through feedback, the loop forces the phase of the signal source to track the phase of the feedback signals;” should be replaced with "Through feedback, the loop forces the phase of the feedback signals to track the phase of the signal source;" (ph)

Page 67 before (3.57) the nominal phase is π/2 not π/4, and thus, one can have an additional phase error of π/2. Similarly, the last term in (3.57) should be π/2 (bt)

Page 67 just after (3.57) PDF/CP should be PFD/CP (cp)

Page 71, 72 X-axes labels for Figures 3.25 and 3.26 should be Time (μs), not Time (ms). (jr)

Page 90, Figure 4.3. The input to the flip-flop labeled as $\overline{R}$ should actually be clock. Also, the bottom two nand gates should not both have outputs labeled with R, The top of these should be $\overline{R}$. The correct diagram is given below. (mm)



Page 92 In the full adder equations (4.1) the equation for carry out should be:

$$c\_out = x \cdot y + y \cdot c + x \cdot c\_in$$

and the correct code should be

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assign c_out= (x & y) | (x & c_in) | (y & c_in);
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Fig. 4.5. is correct. (sb)

Page119 The statement “CMOS rail-to-rail logic is differential and, therefore, has good power-supply rejection,” is incorrect. It should be replaced with “CML is differential and therefore, has good PSR.” This is correctly indicated in the table on page 120. (kp)

Page 148 Second last paragraph describing the band gap reference states that the two BJTs are biased at different currents. Instead it should say that the two BJTs are biased at different current densities, but the same current. This results in small changes to the following paragraphs and to (5.54) and (5.55) as follows:

Next, to cancel this negative temperature/voltage relationship, a voltage that increases with temperature must be found. To do this, assume that two BJTs are biased at different current densities, but the same current. Then the difference between their base-emitter voltages will be given by:

$$\Delta V = V_{BE1} - V_{BE2} = \frac{kT}{q}\ln\frac{I_C}{I_{S1}} - \frac{kT}{q}\ln\frac{I_C}{I_{S2}} = \frac{kT}{q}\ln\frac{I_{S2}}{I_{S1}} = \frac{kT}{q}\ln N \qquad (5.54)$$

Since (5.54) does not have I_S in it, this relationship is much simpler than (5.52) and this voltage is directly proportional to temperature. In this case, the slope of the temperature dependence is given by:

$$\frac{d\Delta V}{dT} = \frac{k}{q}\ln\frac{I_{S2}}{I_{S1}} = \frac{k}{q}\ln N \qquad (5.55)$$

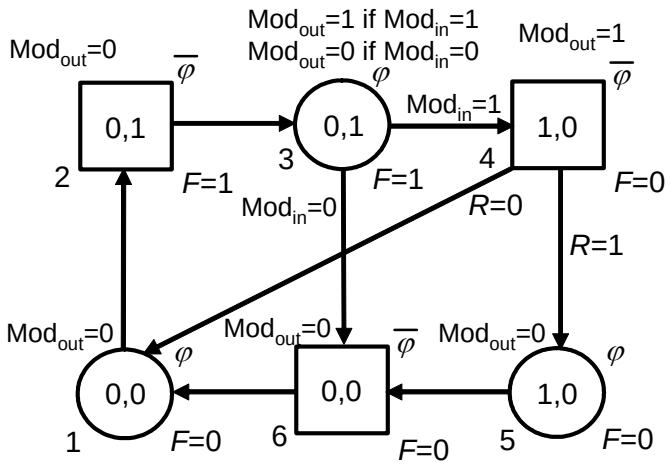
Therefore, the slope can be adjusted by changing N, the ratio of size of Q_1 and Q_2, and, by proper choice, can be made equal in magnitude and opposite in sign to (5.53). (jr)

Page 90 Diagram for flip flop should have “clock” instead of “Rbar” as input. (mm)

Page:157, Lines:3-5 statements of clock high and low should be exchanged, that is the sentence should read “If the clock is low, the next state is the inverse of the current state, and if the clock is high, then the next state is simply equal to the current state”. (mu)

Page:159, Last paragraph, line: 1-2 "Tables 6.5 through 6.11" should be "Tables 6.5 through 6.10". It makes them six tables as mentioned in the previous line. Table 6.11 is only mentioned on Page 163. (mu)

Page 166, Updated Figure 6.13 is shown below. Corrections have been made to the label at top center “Mod_{out} =0 if Mod_{in} = 0”. Also state labels 1 through 6 (starting with 1 on bottom left and increasing clockwise around the figure) have been added. (bt, jr)

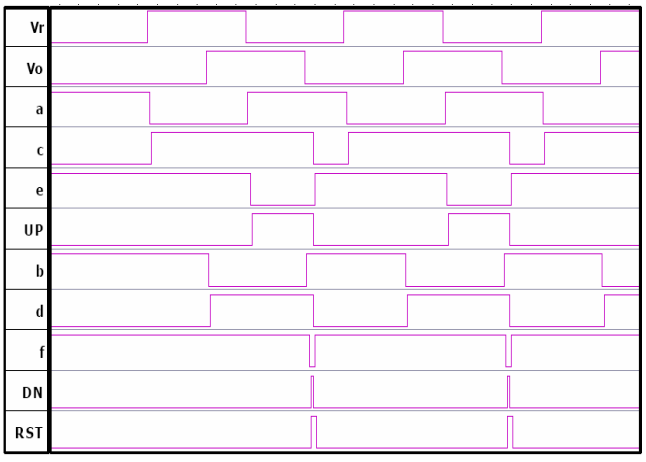


Page 167, Figure 6.15, signals labeled Q1 and Q2 should instead be the outputs of latches Q2 and P2. Also, the signal 2/3 should go low for one full clock cycle, that is, it changes only on the falling edge of the clock and should be triggered from MOD_{out}, not directly from the output of latch P2 (jr).

Page 168, Figure 6.17, the signal labeled Mod_1 should be Mod_0, the signal labeled Mod_2 should be Mod_1 and the input on the right labeled High is Mod_2. This brings the figure into alignment with the text and with the following diagrams. (mu)

Page 185 Fig 6.41. The input V_R and DN2 are reversed. That is, DN2 should be connected to the inverting input, while V_R should be connected to the noninverting input. (jr)

Page 191, 192, At the top left of the modified tri-state PFD is a nand gate with v_R as an input and *a* as the output. Whenever an input to a nand gate is low, the output must be high, yet in the plots on page 192, sometimes v_R and *a* are both low. Similarly, in the bottom gate, when v_o is low, *b* must be high, but again the plot shows times when both are low. The schematic is correct, but the output plots are in error. The correct output plot should be as shown below.



Page 254, Near top of page, the calculation of B, the result given as 0.885565 rad/s should be 0.0885565 rad/s. The result in Hz, given as 0.014096 Hz is correct. (cp)

Page 256, Figure 8.21, call outs on the figures should be for current in μA, not mA. The caption and surrounding text are correct. (cp)

Page 274 Two equations for calculating the currents have come from page 245, but have been inverted, and each equation has an extra factor of I that should not be there, and the second equation also has an extra factor of $v_{out}|_{SE}$. The resulting currents are correct as shown. The correct equations should be:

$$I_{Comp} = \frac{\pi \cdot v_{out}\big|_{Comp}}{2R_p} = 3\,\text{mA}, \quad I_{PMOS} = \frac{\pi \cdot v_{out}\big|_{PMOS}}{R_p} = 12\,\text{mA}$$ (ys)

Page 324 Figure 9.21, In the main path, z^{-1} blocks are shown directly in series with the quantizer outputs. Instead these z^{-1} blocks should be in the feedback paths. That is, the quantizer output should go directly to the summing block for the next stage in addition to going to the z^{-1} block in the feedback. The equations on page 325, that is (9.45), (9.46) and (9.47) are correct for the corrected figure. (nw)

Page 342 Fig 9.39. In the blow up, numbers between 0 and 0.1 on the horizontal axis were each missing a zero – they should be 0.02, 0.04, 0.06, and 0.08. (bt)

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Frequency synthesizers are used in everything from wireless and wireline communications to waveform generation, but until now circuit design expertise in this area has been scattered in numerous trade publications and papers. This one-stop resource gives circuit designers all the straight-from-the-lab techniques, procedures, and applications they need for their work in the field.Â Library of Congress Cataloging-in-Publication Data Rogers, John (John W. M.) Integrated circuit design for high-speed frequency synthesis / John Rogers, Calvin Plett, Foster Dai. p. cm.â€”(Artech House microwave library) Includes bibliographical references and index. ISBN 1-58053-982-3 (alk. paper) 1. Very high speed integrated circuitsâ€”Design and construction. I. Plett, Calvin. II. Advanced Phase-Lock Applications: Frequency Synthesis. James A. Crawford. Â©2010-2011 James A Crawford AM1 LLC.Â Ð‡ High-speed frequency or phase switching Ð‡ Wideband phase and or frequency modulation capability Ð‡ Phase linearity and continuity Ð‡ Linear frequency sweeping. With the availability of very high performance 12- and 14-bit DACs now, the range of applications where direct digital synthesis is a viable alternative has increased substantially.Â In general though, many factors influence the final design decisions. A grade-card to facilitate some of the performance tradeoffs is provided in Table 5-1. Table 5-1 Direct Digital Synthesis Compared to Alternative Synthesis Methods.